A Four-level π-type Converter for Low-voltage Applications

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Keywords

«Multilevel converters», «Converter circuit», «Converter control», «Modulation Strategy».

Abstract

This paper has introduced a four-level π-type converter for low-voltage applications which has a simple structure with six switches per phase leg. The line output voltage has seven levels and the output harmonics is much lower than the conventional two-level converter. The switching states and their associated output voltage levels have been analyzed. A simple carrier-based modulation method with zero-sequence signal injection has been devised to modulate the converter and regulate dc-link neutral points' voltages. The two neutral points' voltages can be well controlled with a back to back configuration even under high modulation index and high power factor. Simulation and experimental results have validated the topology, modulation and control strategy for the four-level π-type converter.

Introduction

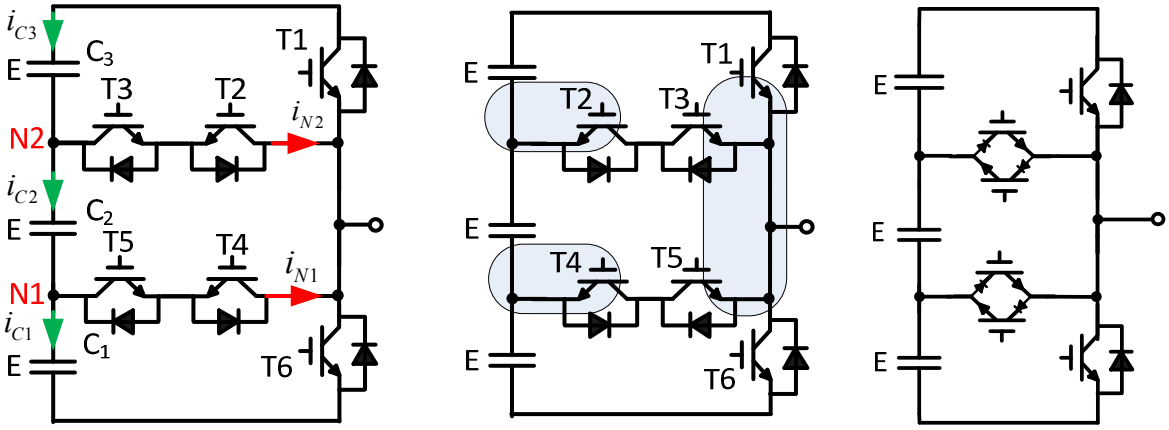
Multilevel converters are commonly used in medium voltage (3~33kV) high power applications. Nevertheless, they are recently widely considered in low-voltage (200~460V) applications as an alternative to the conventional two-level converter [1]. Thanks to the reduced output harmonics of a multilevel converter, compared with a two-level converter, to achieve the equivalent output harmonics, the switching frequency of the multilevel converter can be kept low, thus reducing the switching losses and shrinking the heatsink size. On the other hand, if operated at the same switching frequency, the filter size of the multilevel converter can be smaller. Either way will improve the system power density, which is favoured in more electric aircrafts, electric/hybrid vehicles, solar or wind power generation, where converter size and weight is an important factor. In addition, the switching loss of multilevel converters is generally lower than the two-level converter due to the use of lower voltage-rating devices and lower switching voltage [2]. This means the efficiency drops slowly with the increase of the switching frequency, which provides the possibility to further increase the switching frequency and achieve a higher power density.

Although the output harmonics can be further reduced with converters of higher number of voltage levels, e.g. four-level or five-level, the main concern is the increased complexity regarding the circuit (e.g. number of devices, gate drive, etc) and control complexity (modulation, capacitor voltage balancing, etc) [3]. In this paper, an alternative four-level π-type converter is introduced with only six switching devices per phase leg. Furthermore, only two additional gate drive power supplies are needed in addition to the power supplies required by the conventional two-level converter. This topology does not need the clamping diode or flying capacitor as required in the diode neutral-point-

clamped (NPC) converter or flying capacitor converter, which simplifies the circuitry. A critical issue of this topology is the balancing of the dc-link capacitors' voltages. If a single-end converter is used, e.g. rectifier or inverter, the dc-link capacitors' voltages can not be balanced under high modulation index and high power factor. However, if a back-to-back structure is used, with proper control, the capacitors' voltages can be balanced. This paper has developed a simplified algorithm for modulation and capacitors' voltage balancing of the four-level π-type converter.

Converter topology

Fig.1 (a) shows the phase-leg structure of a four-level π-type converter, which has six switching devices (e.g. IGBTs or MOSFETs). T1 and T6 are the same as in a conventional two-level converter and need to withstand the whole dc-link voltage. Two bidirectional current flow paths have been created between the dc-link neutral points (N1 and N2) and the phase output. Two IGBTs connected back-to-back are adopted to achieve this purpose. In Fig.1 (a), T3 and T4 need to withstand 2/3 of the dc-link voltage (2E). T2 and T5 only need to withstand 1/3 of the dc-link voltage (E). With this configuration, the phase leg can output four voltage levels, i.e. dc-link voltage (3E), 2/3 of the dc-link voltage (2E), 1/3 of the dc-link voltage (E) and zero (0).



(a) (b) (c)

Fig.1. A four-level π-type converter phase leg with different device configurations: (a) with back-to-back IGBTs of common emitter connection as center legs, (b) with back-to-back IGBTs of common collector connection as center legs, (c) with reverse blocking IGBTs as centre legs.

Regarding the device voltage ratings, for a 600V dc-link voltage, T1 and T6 can normally be 1200V devices (e.g. IGBTs) to leave 600V voltage margin. On the other hand, during transient (commutation), the voltage across T1 or T6 will be clamped to the neutral points, i.e. N2 or N1. Therefore, the voltage across T1 or T6 during transient will only be E (200V) plus the voltage drop across the parasitic inductance. Hence, T1 and T6 need to withstand 600V in static and 200V plus voltage drop of the parasitic inductance during commutation (e.g. < 600V). This means only a small voltage margin is actually needed for T1 and T6. For example, 900V super-junction MOSFETs may be suitable for this purpose. Similarly, T3 and T4 need to withstand 400V in static and 200V plus the parasitic voltage drop during commutation. 600V IGBTs or MOSFETs may be used. For T2 and T5, the devices need to withstand 200V in static and 200V plus the parasitic voltage drop during commutation. Therefore, 400V devices can be used.

Table I: Device voltage ratings and candidate devices

	T1, T6	T3, T4	T2, T5
Minimum device voltage rating	900V	600V	400V
Candidate devices	1200V IGBT or 900V Super-junction MOSFET	600V IGBT or 600V MOSFET	600V IGBT or 400V MOSFET

In terms of the required gate driver power supply, as shown in Fig.1 (a), T2 and T3, with common emitter connection can share the same gate drive power supply, so as for T5 and T4. Therefore, 6 additional isolated gate driver power supplies are needed for a three-phase four-level π-type converter compared with the conventional two-level converter. Alternatively, the two back-to-back IGBTs can be connected in a common collector configuration as shown in Fig.1 (b), where T1, T3 and T5 can share the same gate driver power supply. T2 and T4 need two separate gate power supplies, which can be shared by all the three phase legs. In total, only two more gate power supplies are needed for a three-phase four-level converter in addition to the ones used for a conventional two-level converter. The topology can be further simplified by using reverse-blocking IGBTs (RB-IGBTs) as shown in Fig.1(c). In this way, the conduction loss of the converter can be further reduced by eliminating the diode in the neutral conduction paths.

Fig.2 shows the converter output voltage levels and the corresponding conductive devices according to the current direction. To guarantee successful commutation from one level to another adjacent level, especially during dead-time period, one device must be kept "ON" in both the two levels. For example, switching from 3E to 2E as shown in Fig.2 (a) (b), T3 should be always "ON". T1 and T2 switch ON and OFF in a complementary fashion. When the output voltage demand is 3E, T1 is turned ON. When the output voltage demand is 2E, T2 is turned ON. Assuming the current flows out of the converter, for the 3E voltage level, the current flows through T1 and for the 2E level, current flows through D2 and T3. During dead-time, the current flows through D2 and T3 as well. Table II shows the device switching states and the corresponding output voltage levels. T1 and T2, T3 and T4, T5 and T6 switch in a complementary manner. Note that since the output voltage only switches between adjacent voltage levels with one voltage step (E), the switching voltage for each device (T1~T6) is E (e.g. 200V for a 600V dc-link voltage), which reduces the switching loss. In contrast, in a conventional two level converter, the devices need to switch the full dc-link voltage.

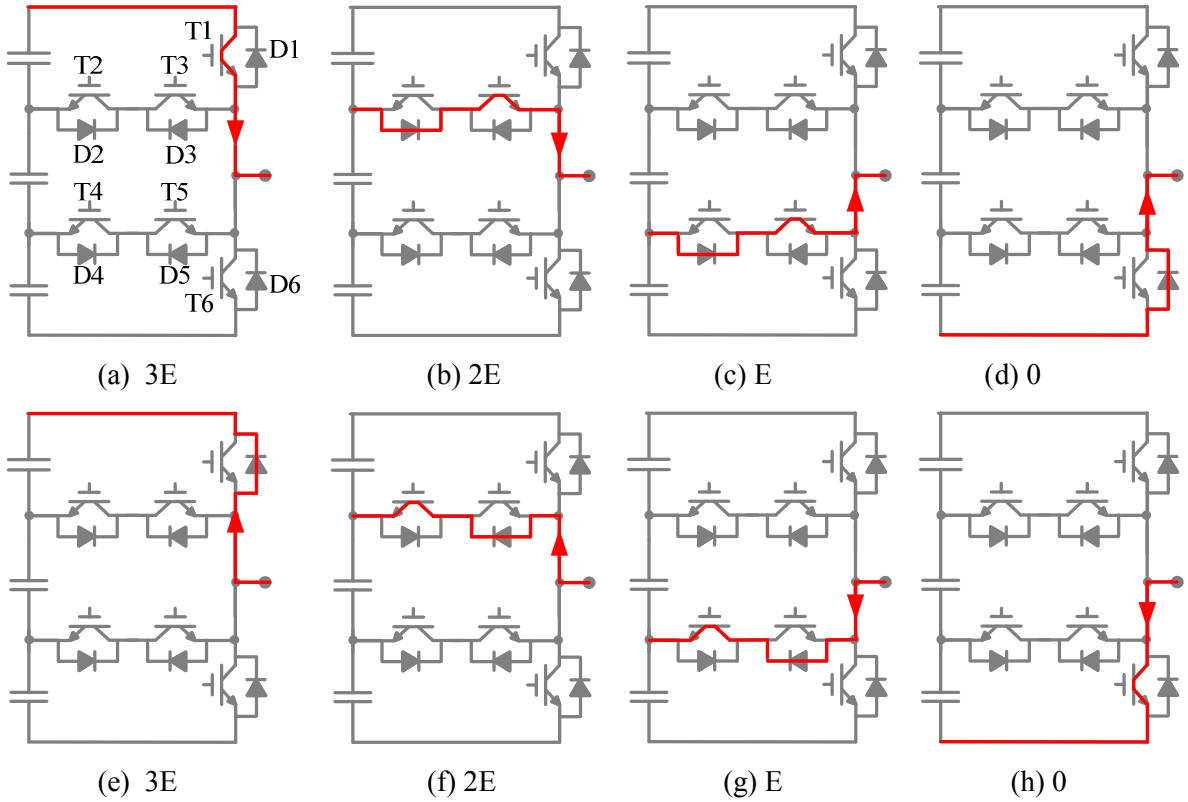


Fig.2. Switching states and current flow path: (a)~(d) current flows out of the converter; (e)~(h) current flows into the converter

Table II. Switching states and output voltage levels

Device / Voltage level	T1	T2	T3	T4	T5	T6
3E	ON	OFF	ON	OFF	ON	OFF
2E	OFF	ON	ON	OFF	ON	OFF
E	OFF	ON	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON	OFF	ON

Modulation and dc-link capacitors' voltage control

Similar as in a two-level converter, the modulation of a four-level converter can use space vector modulation (SVM) or carrier-based modulation [3]. SVM can be used to balance the dc-link capacitors' voltages (neutral points' voltages) through the selection of redundant vectors. For a four-level converter, the total number of space vectors is 64 and the selection of voltage vectors, calculation of the time duration of each vector and the arrangement of the sequence of each vector become very complicated and computationally intensive. On the other hand, the equivalence between carrier-based modulation and SVM has been proved in [4, 5]. The carrier-based modulation can greatly simplify the modulation process if the desired modulation signals can be identified. In the following, a carrier-based modulation method with optimized zero-sequence signal injection is presented to modulate the switches and at the same time to balance the neutral point voltages of the four-level π-type converter.

The reference voltage (modulation signal) for the converter is composed of two parts: fundamental components (three-phase sinusoidal) and a zero-sequence component as given in (1).

$$u_i(t) = u_i^*(t) + c(t) \qquad i = a, b, c \tag{1}$$

Where, $u_i(t)$ is the reference voltage; $u_i^*(t)$ are the fundamental components; $c(t)$ is the zero-sequence component. The fundamental components are obtained from the output of the current control loop, which are used to control the fundamental current of the converter to track the reference. The zero-sequence component can be adjusted and added to the three-phase fundamental components simultaneously to achieve neutral points' voltage balancing. If the phase reference voltage is normalized with 1/3 of the dc-link voltage (e.g. E in Fig.1), then the per unit value of the phase reference voltage with regard to the negative dc-bus will be in the range of 0~3. Therefore, the maximum and minimum zero-sequence component $c(t)$ that can be added to the fundamental components can be expressed as

$$-u_{\min}^*(t) \le c(t) \le 3 - u_{\max}^*(t) \tag{2}$$

Where, $u^*_{\max}$ and $u^*_{\min}$ are the maximum and minimum value of the three-phase fundamental components, as are given by

$$\begin{cases} u_{\min}^*(t) = \min(u_a^*(t), u_b^*(t), u_c^*(t)) \\ u_{\max}^*(t) = \max(u_a^*(t), u_b^*(t), u_c^*(t)) \end{cases} \tag{3}$$

After the available range of zero-sequence signal is derived by (2), the optimized zero-sequence signal can be selected from it. Although the optimized zero-sequence signal for capacitor voltage balancing may be derived analytically, it would be much simpler to just sample several values within the range given in (2). For example, ten values can be selected equally within the range given in (2) and evaluated against the control objective, e.g. neutral point voltage balancing. And the one which leads to the optimized value of the control objective will be selected. In order to balance the dc-link capacitors' voltages, the control objective can be set to minimize the capacitor energy J as given in (4) [6, 7].

$$J = \frac{1}{2} C \sum_{j=1}^{3} \Delta v_{Cj}^2 = \frac{1}{2} C \sum_{j=1}^{3} (v_{Cj} - \frac{V_{dc}}{3})^2 \tag{4}$$

Where, Δv_{Cj} is the voltage deviation of capacitor C_j in Fig.1(a) from 1/3 of the dc-link voltage. v_{Cj} is the capacitor voltage. V_{dc} is the dc-link voltage. C is the capacitor value. If an optimized zero-sequence signal is selected, J can be minimized (ideally reduced to zero) when the capacitors' voltages are regulated at the reference value of 1/3 of the total dc-link voltage. The condition to obtain a minimum value for J is

$$\frac{dJ}{dt} = C\sum_{j=1}^{3}\Delta v_{Cj}\frac{dv_{cj}}{dt} = \sum_{j=1}^{3}\Delta v_{Cj}i_{Cj} \le 0 \tag{5}$$

Where, i_{Cj} is the current flowing through the capacitor C_j. Therefore, the control objective can be set as in (6) and the control variable is the zero-sequence component with the defined range in (2).

$$\begin{cases} \min V = \sum_{j=1}^{3}\Delta v_{Cj}i_{Cj} = \sum_{j=1}^{3}(v_{Cj} - \frac{V_{dc}}{3})\cdot i_{Cj} \\ \text{Constriant}: \quad -u^{*}_{\min}(t) \le c(t) \le 3 - u^{*}_{\max}(t) \end{cases} \tag{6}$$

The next step is to find out the relationship between the control objective and zero-sequence signal so that each zero-sequence signal can be evaluated against the control objective.

The relationship between capacitor current i_{Cj} in (6) and the neutral point currents i_{N1}, i_{N2} can be derived according to Fig.1 (b) and is given in (7).

$$\begin{cases} i_{C1} = -\frac{1}{3}i_{N2} - \frac{2}{3}i_{N1} \\ i_{C2} = -\frac{1}{3}i_{N2} + \frac{1}{3}i_{N1} \\ i_{C3} = \frac{2}{3}i_{N2} + \frac{1}{3}i_{N1} \end{cases} \tag{7}$$

Since the reference voltage has been normalized within the range of 0~3, the integer part of the voltage reference (u_i) represents the voltage level and the fractional part determines the duty cycle. This significantly simplifies the calculation to find out the relationship between neutral point currents, modulation signal and phase current. For example, if the reference voltage is 1.2, it means the voltage level is 1 and the duty cycle is 0.2. Therefore, the output voltage will switch between E and 2E. Specifically, the output voltage will be E for 80% of the switching period with switches T4 and T5 ON, where the phase output current flows through i_{N1}. The output voltage will be 2E for 20% of the switching period with switches T2 and T3 ON, where the phase current flows through i_{N2}. Therefore, the neutral currents (i_{N1}, i_{N2}) can be determined by the reference voltage level (integer part of the reference voltage) and the duty cycle (fractional part of the reference voltage). The illustration of the voltage level and duty cycle with regards to the integer and fractional part of the reference voltage is shown in Fig.3.

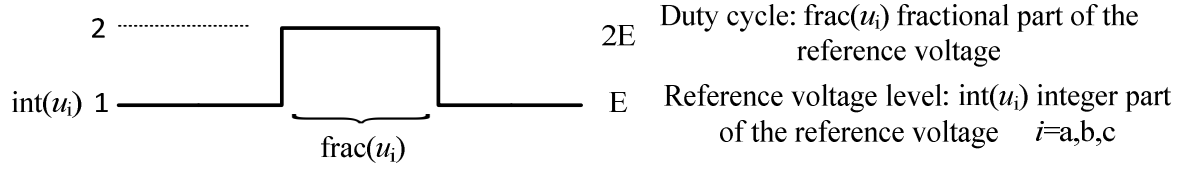


Fig.3. Illustration of the reference voltage level and duty cycle (u_i=1.2)

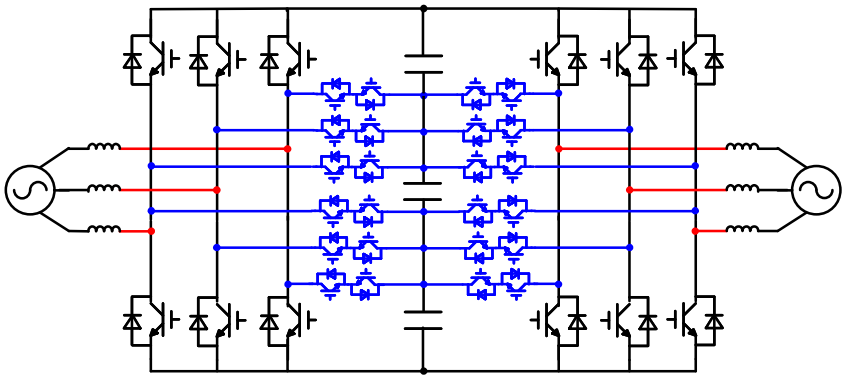
Note that the reference voltage u_i can be adjusted by the zero-sequence component, which explains why the zero-sequence component can affect the neutral current, the corresponding capacitor current and the control objective in (6). The relationship between the neutral point current and the reference voltage (including zero-sequence voltage) can be formulated as in (8) [5].

$$\begin{cases} \overline{i}_{N1} = \sum\limits_{i=a,b,c} i_i \times \left[(\text{int}(u_i) == 0) \times \text{frac}(u_i) + (\text{int}(u_i) == 1) \times (1 - \text{frac}(u_i)) \right] \\ \overline{i}_{N2} = \sum\limits_{i=a,b,c} i_i \times \left[(\text{int}(u_i) == 1) \times \text{frac}(u_i) + (\text{int}(u_i) == 2) \times (1 - \text{frac}(u_i)) \right] \end{cases} \tag{8}$$

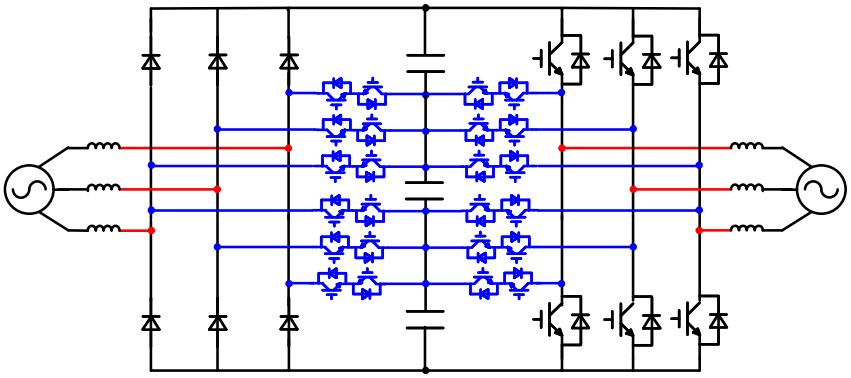
Where, int(u_i) represents the integer part of the reference voltage, frac(u_i) represents the fractional part of the reference voltage. i_a, i_b, i_c are the converter phase currents. int(u_i)= =0 is used to check whether the reference voltage level is 0 or not. If it is zero, then (int(u_i)==0) equals to 1, otherwise 0. It can be seen that only when the voltage level is 0 or 1, the phase current may flow through i_{N1}. When the voltage level is 1 or 2, the phase current may flow through i_{N2}.

With the above equations (1)-(8), the relationship between the control objective and the zero-sequence signal can be established. In summary, the modulation and neutral point voltage balancing algorithm can be implemented as follows. Firstly, the three-phase fundamental components are obtained from the current control loop. Secondly, using (2), the range of zero-sequence component can be derived. Thirdly, equally sample several values within the range of the zero-sequence component, and adds to the fundamental component to obtain the reference voltage. Fourthly, using (8), (7) to check which zero-sequence component leads to the minimum value of the objective function in (6). That zero-sequence component will be selected to form the final reference voltage. After the reference voltage is obtained, it will be compared with three triangle carrier-signals to generate the PWM signals for the device gate drivers.

It should be noted that although the above algorithm attempts to balance the neutral points' voltages, it can only balance them under low modulation index or low power factor conditions but not with high modulation index and high power factor unless a back-to-back structure is employed. With a back-to-back structure, the current/power flowing through the neutral points (N1 and N2) can be coordinated [6-8]. Fig.4 shows the four-level back-to-back π-type converter structures. Fig.4 (a) can allow bi-directional power flow, which can be used, for example, in motor drive applications where there is regenerative power requirement. Fig.4 (b) shows the configuration for unidirectional power flow, where the front-end six main switches are replaced with diodes. This may reduce the system cost and can be used in applications such as aircraft generator/converter system or wind power generation system, where the power flows in only one direction.



(a)



(b)

Fig.4. Back-to-back four-level π-type converter structure. (a) Bidirectional power-flow structure, (b) unidirectional power flow structure

With the back to back four-level π-type converter, the neutral points' voltage balancing needs to be implemented at both the rectifier and inverter side. This can be done through two separated controllers for rectifier and inverter control respectively. A local optimized zero-sequence signal will be selected to balance the dc-link neutral points at the rectifier and inverter side. Alternatively, a single controller can be used to achieve an overall optimization by selecting the best zero-sequence based on the information from the rectifier and inverter side together. If a single controller is used, the calculation of the neutral point current and capacitor current should consider both the rectifier and inverter current and reference voltage.

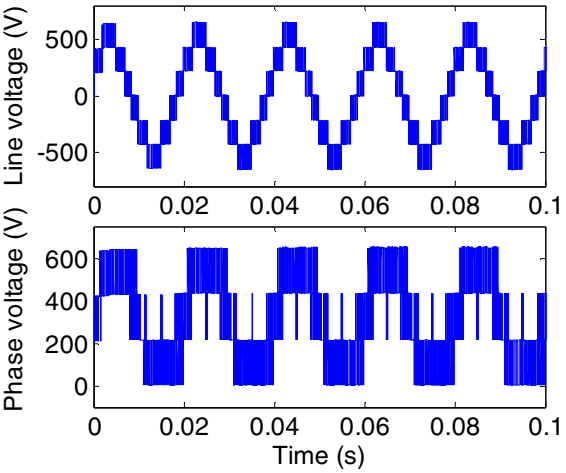
Simulation results

A simulation system has been set up in MATLAB/Simulink with the configuration shown in Fig.4 (a) in order to validate the topology, control and modulation. The input to the converter (rectifier) is a three-phase grid and the output of the converter (inverter) is connected to a three-phase R-L load. The rectifier control loop consists of outer dc-link voltage loop and inner current loop. The inverter side operates under open loop control with a voltage reference. The grid line voltage is 300V, the load side line voltage is 342V and the dc-link voltage is 650V. This will give a modulation index of 0.9 at both the rectifier side and inverter side. The rectifier-side power factor is 1 and the load-side power factor is close to 1 as well. The switching frequency is 10kHz.

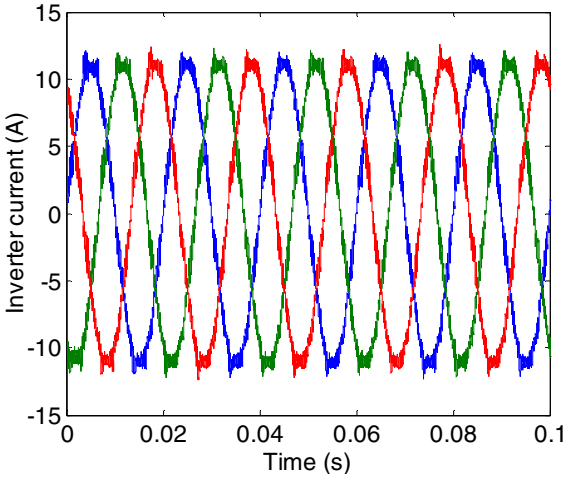
Fig.5 shows the simulation results. Fig.5 (a) shows the inverter output line voltage and phase voltage. The line voltage has seven levels and the phase voltage has four levels. As seen, there are some distinct pulses appearing in the phase output voltage, which is due to the adding of optimized zero-sequence component for dc-link neutral points' voltage regulation. As expected, these pulses do not appear in the line voltage due to the cancellation of zero-sequence component between phases. Fig.5 (b) shows the three-phase sinusoidal load currents. There are switching harmonics appearing in the current waveform, which is due to the high power factor and relatively small inductor. Fig.5(c) shows the three dc-link capacitor voltages, which are well regulated around a third (216.7V) of the total dc-link voltage of 650V. The initial capacitor voltage is set at 210V to check the transient response of the controller with a recovery to the reference voltage of 216.7V. It can be seen that voltages of the upper and lower capacitors are very close to each other. The middle capacitor voltage has slight deviation from the upper and lower capacitors. This can be clearly seen in a detailed waveform in Fig.5 (d). Fig.5 (e) shows the total converter dc-link voltage which is regulated at 650V by the rectifier. The initial dc-link voltage is set as 630V. Fig. 5(f) shows the grid voltage and current under unity power factor operation. As seen, the grid current is sinusoidal and in phase with the grid voltage.

Several other scenarios have also been tested in simulation as well. It has been found out using a single controller for the rectifier and inverter with an overall optimized zero-sequence signal has better control of the dc-link neutral points than two separate controllers for respective rectifier and inverter with locally optimized zero-sequence signals. In the simulation results shown in Fig.5. The modulation index is 0.9 under unity power operation. If a higher modulation index is demanded, e.g. 0.95 or 1, the neutral points voltages start to diverge. This can be understood by the fact that with higher

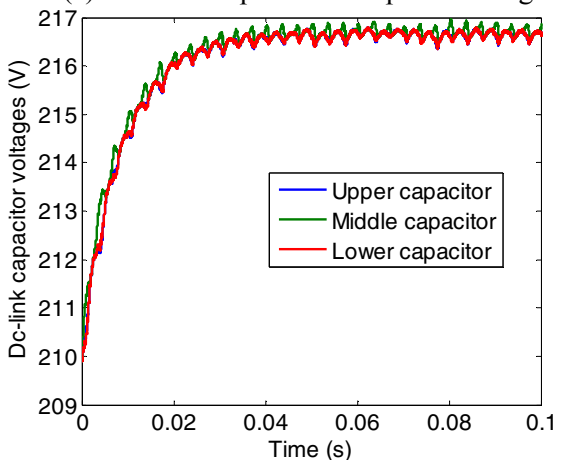
fundamental voltage, the freedom for zero-sequence signal selection given in (2) is less. Therefore, the controllability of the neutral points' voltage is limited.



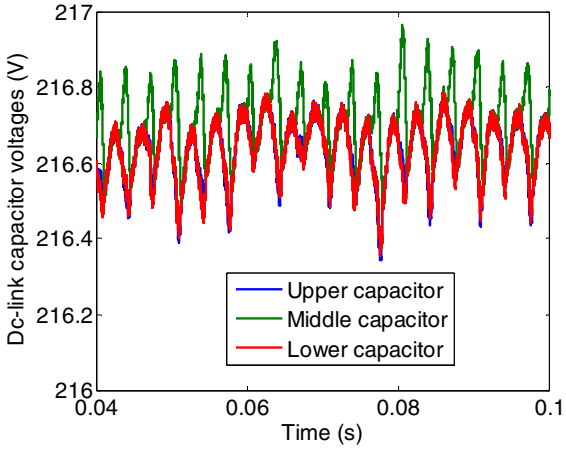
(a) Inverter output line and phase voltage



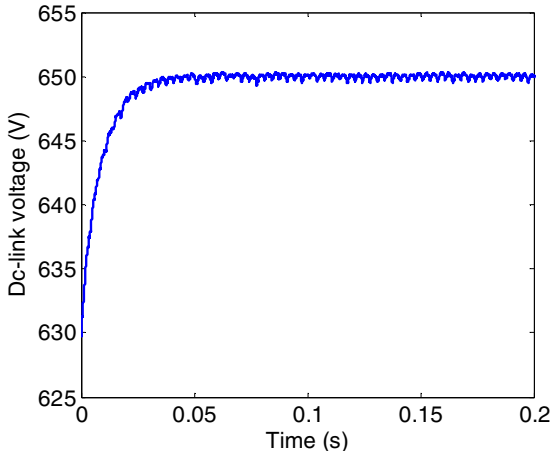
(b) Inverter load current



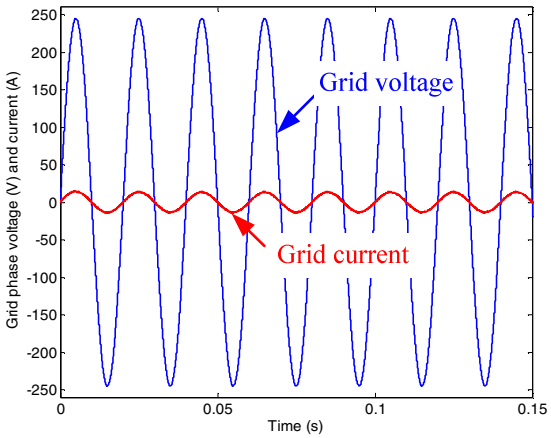
(c) Three dc-link capacitor voltages



(d) Detailed waveform of the capacitor voltages



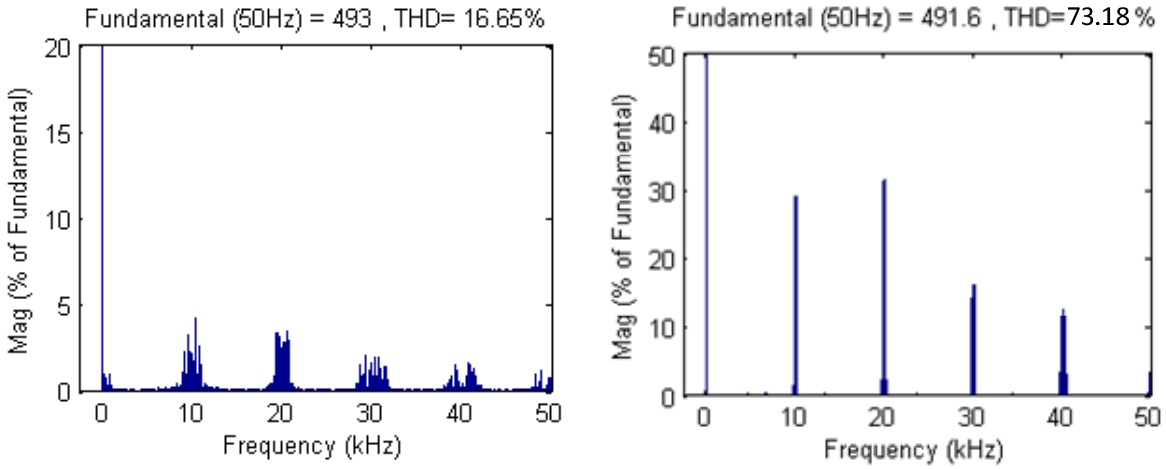
(e) Total dc-link voltage



(f) Grid voltage and current

Fig.5. Simulation results with a back-to-back four-level π-type converter

Fig.6 further shows the output voltage harmonics comparison between two-level and four-level converters. The switching frequency is 10kHz. As seen, the switching harmonics of a four-level converter is much lower than a two-level converter as well as the total harmonic distortion (THD). This means the required output filter or EMI filter for a four-level converter can be smaller than a two-level converter.

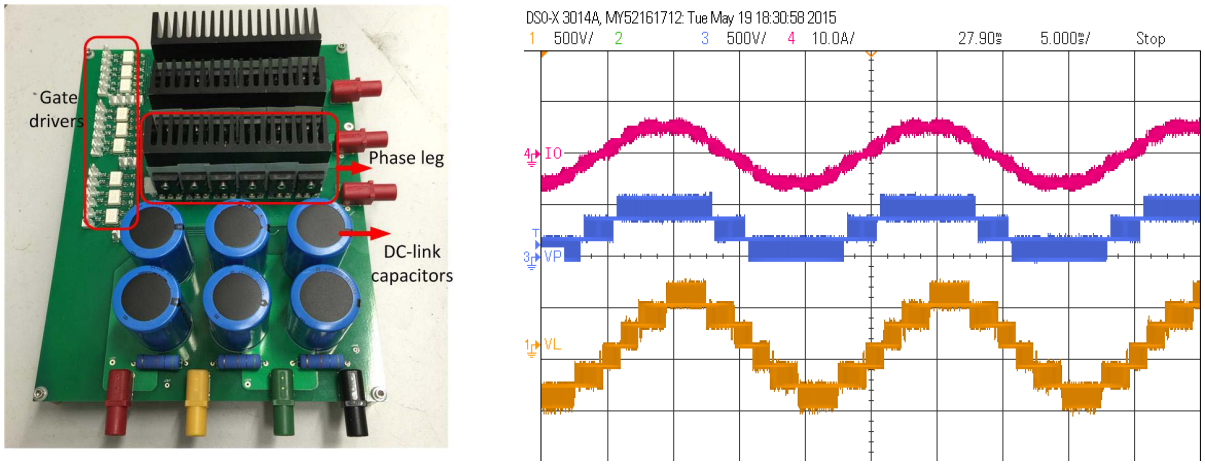


(a) Four-level converter (b) Two-level converter

Fig.6. Harmonics comparison

Experimental results

An experiential prototype was built to test the performance of the four-level π-type converter as shown in Fig.7 (a). In the experiment, the three dc-link capacitor voltages are clamped to 200V by three independent power supplies, giving a total dc-link voltage of 600V. A three-phase inductor (50μH) and resistor (44Ω) load is used. An open-loop sinusoidal carrier-based modulation is used to generate the PWM waveforms with a modulation index of 0.95. Fig.7 (b) shows the phase voltage (four levels), line voltage (seven levels) and the load current under 50 kHz switching frequency and 95.3% efficiency is achieved.



(a) (b)

Fig.7. (a) Experimental prototype; (b) Experimental waveforms: (1) line voltage, (3) phase voltage (with reference to negative dc-link), (4) load current.

Conclusion

This paper has introduced a four-level π-type converter, which can be a good candidate for low voltage applications in terms of reduced harmonics and improved power density. The new topology only requires two additional gate driver power supplies compared with the standard two-level converter. With the modulation scheme presented in the paper, the modulation process for the four-level converter can be greatly simplified compared with the conventional space vector modulation. In addition, the neutral point' voltages can be well controlled with a back to back structure even under high modulation index and high power factor conditions.

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